AMENDMENT TO THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims.

Listing of Claims

1. (Currently Amended) A method of designing a semiconductor interconnect architecture including a pair of metal layers interconnected by a plurality of conductive vias, the method comprising:

determining via stress as a function of a via density, the via density being a ratio of the plurality of conductive vias interconnecting the pair of metal layers to an area of the pair of metal layers;

identifying a ~~via-to-metal area ratio~~ via density value below which the stress on a via does not significantly increase relative to the stress on the via above the via density value; and

~~requiring~~ positioning the plurality of conductive vias in the semiconductor interconnect architecture according to ~~have~~ a ~~via-to-metal area ratio~~ via density being at least as large as said via density value.

2. (Original) The method of Claim 1, wherein said value is approximately 1/100.

3. (Original) The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

4. (Original) The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

5. (Original) The method of Claim 2, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.

6. (Currently Amended) A method of producing a semiconductor interconnect architecture, the method comprising:

providing a first metal layer;

providing a second metal layer; and

providing a plurality of conductive vias interconnecting said first and second metal layers ~~and achieving~~;

determining via stress as a function of a via density, the via density being a ratio of the plurality of conductive vias interconnecting the first metal layer and the second metal layer to an area occupied by the first metal layer and the second metal layer; and

positioning the plurality of conductive vias in the semiconductor interconnect architecture according to a via-to-metal area ratio being at least as large as a predetermined via-to-metal area ratio value below which the stress on the vias does not significantly increase relative to the stress on the vias above the value.

7. (Original) The method of Claim 6, wherein said value is approximately 1/100.

8. (Original) The method of Claim 7, wherein each of said plurality of conductive vial has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

9. (Original) The method of Claim 7, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

10. (Original) The method of Claim 7, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.

11. (Currently Amended) A semiconductor interconnect architecture, the architecture comprising:

a first metal layer;

a second metal layer; and

a plurality of conductive vias interconnecting said first and second metal layers, said vias ~~and said metal layers cooperable to provide~~ arranged with respect to the first metal layer and the second metal layer according to a via-to-metal area ratio being at least as large as a predetermined via-to-metal area ratio value below which stress on the plurality of vias does not significantly increase relative to stress on the vias above the value.

12. (Original) The semiconductor interconnect architecture of Claim 11, wherein said value is approximately 1/100.

13. (Original) The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.04 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.25 via/μm^2.

14. (Original) The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.03 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.3 via/μm^2.

15. (Original) The semiconductor interconnect architecture of Claim 12, wherein each of said plurality of conductive vias has a cross-sectional area of approximately 0.02 μm^2 and said semiconductor interconnect architecture has a via density of approximately 0.44 via/μm^2.